AMENDMENTS

In the Specification:

Amend paragraphs [0005] and [0006] as follows:

[0005] A gate line 11 extending in the column direction is connected to a gate of the pixel selection transistor, and a drain line 12 extending in the row direction is connected to a drain of the transistor. A vertical scanning signal is consecutively supplied from a shift ~~resister~~ register 13 of a vertical scanner to the gate line 11 of each column, and the pixel selection transistor is selected accordingly.

[0006] The RGB display data of the first row is stored in a ~~resister~~ register 21-1 and inputted to a DA converter 23-1 at the first row based on a horizontal scanning signal from a shift ~~resister~~ register 20-1 of a horizontal scanner. A γ-correction voltage of the DA converter 23-1 is supplied from a γ-correction voltage generating circuit 24. The output from the DA converter 23-1 is supplied to the drain line 12 through an amplifier 25-1 and written into the selected RGB pixel of the first row. The same applies to the second, third, --- rows. Therefore, the explanation is omitted.

Amend paragraphs [0011] and [0012] as follows:

[0011] The operation of the display device described above is now explained by referring to an operation timing chart of FIG. 8. Horizontal starting pulses HST are shifted by the shift ~~resisters~~ registers 20-1, 20-2, 20-3, and the horizontal scanning signals S/R 0-2 is consecutively generated. The RGB display data that is consecutively sent based on the horizontal scanning signal is then stored in the ~~resisters~~ registers 21-1, 21-2, and 21-3.

[0012] The RGB display data outputted from the ~~resisters~~ registers 21-1,21-2, and 21-3 is then converted into an analog signal by the DA converters 23-1, 23-2 and 23-3 and the γ-correction is simultaneously performed to the analog signal based on the γ-correction voltage

from the γ-correction voltage generating circuit 24. The analog signal is then written into each of the selected RGB pixels through the drain line 120.

Amend paragraphs [0026] - [0030] as follows:

[0026] A gate line 110 extending in the column direction is connected to a gate of the pixel selection transistor, and a drain line 120 extending in the row direction is connected to a drain of the transistor. A vertical scanning signal is consecutively supplied from a shift ~~resister~~ register 130 of a vertical scanner to the gate line 110 of each column, and the pixel selection transistor is selected accordingly.

[0027] The RGB display data inputted parallel based on a horizontal scanning signal from a shift ~~resister~~ register 140-1 of a horizontal scanner is stored in a ~~resister~~ register 141-1 at the first row. The RGB display data inputted parallel based on the horizontal scanning signal from the shift ~~resister~~ register 140-2 of the horizontal scanner is stored in the ~~resister~~ register 141-2 at the second row. The same sequence applies to other rows.

[0028] The RGB display data is taken into each of the ~~resisters~~ registers 141-1, 141-2 --- during one horizontal period. If each RGB of the RGB display data has 6 bits, each of the ~~resisters~~ registers 141-1, 141-2 --- is also configured to store six-bit display data.

[0029] Each of the corresponding RGB display data stored in each of the ~~resisters~~ registers 141-1, 141-2 --- is then outputted during R writing period, G writing period, or B writing period of the following one horizontal period.

[0030] At the first row, the RGB display data outputted from the ~~resister~~ register 141-1 of the first row during the writing period described above is then selected by a switching element 143-1 and inputted to a DA converter 150-1. The DA converter 150-1 is provided with a γ-correction voltage that is generated by a γ-correction voltage switching circuit 160 and outputted for each of the RGB display data based on a R selection signal RSEL, a G selection signal GSEL or a B selection signal BSEL.

Amend paragraph [0041] as follows:

[0041] The operation of the configuration of the display device described above will be explained by referring to a timing chart shown in FIG. 3. Suppose each of the ~~resisters~~ registers 141-1, 141-2, --- has already acquired the RGB display data desirable for each ~~resister~~ register before one horizontal period.

Amend paragraph [0045] as follows:

[0045] Next, the G writing enable signal GENB becomes HIGH after the R writing enable signal RENB changes to LOW. It is the start of the G writing period, and therefore all the G display data is outputted from the ~~resisters~~ registers 141-1, 142-2, --- . Also, only the switching element SW2 of the switching circuit 180 turns on.

Amend paragraph [0048] as follows:

[0048] Next, the B writing enable signal BENB becomes HIGH after the G writing enable signal GENB changes to LOW. It is the start of the B writing period, and therefore all the B display data is outputted from the ~~resisters~~ registers 141-1, 142-2, --- . Also, only the switching element SW3 of the switching circuit 180 turns on.

Amend paragraphs [0058] – [0059] as follows:

[0058] The shift ~~resister~~ register S/R0, the ~~resister~~ register 141-1, a switching element 143-1, the DA converter 150-1, and the amplifier 170-1 for one row are shown in FIG. 4. But the same configuration applied to other rows.

[0059] Next, the operation of the liquid crystal display device of this embodiment will be explained by referring to FIG. 5. Although the following explanation is based on the operation of the first row in FIG. 4 as an example, the same applies to other rows. Suppose the ~~resister~~ register 141-1 has already acquired the desirable RGB display data corresponding to the six pixels before one horizontal period.